CLAIMS

1. (Original) A multiprocessor system comprising:

a first microprocessor having one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock;

a memory controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock; and

a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the memory controller to the second processor, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal, the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time.

2. (Original) The multiprocessor system of Claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus.

3. (Original) The multiprocessor system of Claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus, and wherein the second interfacing logic does not delay the second signal.

4. (Original) The multiprocessor system of Claim 1, wherein the second microprocessor comprises a second interfacing logic connected to the second bus, and wherein

the first interfacing logic delays the first signal by a second period of time and the second interfacing logic delays the second signal by a third period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time.

5. (Original) The multiprocessor system of Claim 1, wherein the memory controller comprises an address switch.

6. (Original) The multiprocessor system of Claim 1, wherein the first and the second signals carry the same data.

7. (Original) The multiprocessor system of Claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-

component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer connected to at least the first and the second storage components for receiving the first and the second storage-component output signals and for generating a third multiplexer output signal, the third multiplexer being controlled by a third control signal; and

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and clocked by a third control clock derived from the first system clock.

8. (Original) The multiprocessor system of Claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal;

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component being clocked by a third control clock derived from the second system clock;

a fourth multiplexer connected to at least the first, the second, and the third storage components for receiving the first, the second, and the third storage-component output signals and for generating a fourth multiplexer output signal, the fourth multiplexer being controlled by a fourth control signal; and

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and clocked by a fourth control clock derived from the first system clock.

9. (Original) The multiprocessor system of Claim 1, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal;

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component being clocked by a third control clock derived from the second system clock;

a fourth multiplexer configured for receiving the first signal and generating a fourth multiplexer output signal and controlled by a fourth control signal;

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and for providing a fourth storage-component output signal to the fourth multiplexer, the fourth storage component being clocked by a fourth control clock derived from the second system clock;

a fifth multiplexer connected to at least the first, the second, the third, and the fourth storage components for receiving the first, the second, the third, and the fourth storage-component output signals and for generating a fifth multiplexer output signal, the fifth multiplexer being controlled by a fifth control signal; and

a fifth storage component connected to the fifth multiplexer for receiving the fifth multiplexer output signal from the fifth multiplexer and clocked by a fifth control clock derived from the first system clock.

10. (Currently Amended) A multiprocessor system comprising:

a memory controller having one or more interfacing logics including a first interfacing logic, the memory controller being clocked by a first system clock;

a first microprocessor connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the first microprocessor to the first interfacing logic, the first microprocessor being clocked by a second system clock; and

a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the second processor to the memory controller, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal, the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the ~~first and the second microprocessors~~ memory controller substantially at the same time.

11. (Original) The multiprocessor system of Claim 10, wherein the memory controller comprises a second interfacing logic connected to the second bus.

12. (Original) The multiprocessor system of Claim 10, wherein the memory controller comprises a second interfacing logic connected to the second bus, and wherein the second interfacing logic does not delay the second signal.

13. (Original) The multiprocessor system of Claim 10, wherein the memory controller comprises a second interfacing logic connected to the second bus, and wherein the first interfacing logic delays the first signal by a second period of time and the second interfacing logic delays the second signal by a third period of time so that the first and the second signals are received by the memory controller substantially at the same time.

14. (Original) The multiprocessor system of Claim 10, wherein the memory controller comprises an address switch.

15. (Original) The multiprocessor system of Claim 10, wherein the first and the second signals carry the same data.

16. (Original) The multiprocessor system of Claim 10, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer connected to at least the first and the second storage components for receiving the first and the second storage-component output signals and for generating a third multiplexer output signal, the third multiplexer being controlled by a third control signal; and

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and clocked by a third control clock derived from the first system clock.

17. (Original) The multiprocessor system of Claim 10, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-

component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal;

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component being clocked by a third control clock derived from the second system clock;

a fourth multiplexer connected to at least the first, the second, and the third storage components for receiving the first, the second, and the third storage-component output signals and for generating a fourth multiplexer output signal, the fourth multiplexer being controlled by a fourth control signal; and

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and clocked by a fourth control clock derived from the first system clock.

18. (Original) The multiprocessor system of Claim 10, wherein the first interfacing logic comprises:

a first multiplexer configured for receiving the first signal and generating a first multiplexer output signal and controlled by a first control signal;

a first storage component connected to the first multiplexer for receiving the first multiplexer output signal from the first multiplexer and for providing a first storage-component

output signal to the first multiplexer, the first storage component being clocked by a first control clock derived from the second system clock;

a second multiplexer configured for receiving the first signal and generating a second multiplexer output signal and controlled by a second control signal;

a second storage component connected to the second multiplexer for receiving the second multiplexer output signal from the second multiplexer and for providing a second storage-component output signal to the second multiplexer, the second storage component being clocked by a second control clock derived from the second system clock;

a third multiplexer configured for receiving the first signal and generating a third multiplexer output signal and controlled by a third control signal;

a third storage component connected to the third multiplexer for receiving the third multiplexer output signal from the third multiplexer and for providing a third storage-component output signal to the third multiplexer, the third storage component being clocked by a third control clock derived from the second system clock;

a fourth multiplexer configured for receiving the first signal and generating a fourth multiplexer output signal and controlled by a fourth control signal;

a fourth storage component connected to the fourth multiplexer for receiving the fourth multiplexer output signal from the fourth multiplexer and for providing a fourth storage-component output signal to the fourth multiplexer, the fourth storage component being clocked by a fourth control clock derived from the second system clock;

a fifth multiplexer connected to at least the first, the second, the third, and the fourth storage components for receiving the first, the second, the third, and the fourth storage-

component output signals and for generating a fifth multiplexer output signal, the fifth multiplexer being controlled by a fifth control signal; and

a fifth storage component connected to the fifth multiplexer for receiving the fifth multiplexer output signal from the fifth multiplexer and clocked by a fifth control clock derived from the first system clock.

19. (New) A system comprising:

a first microprocessor comprising one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock;

a memory controller coupled to the first interfacing logic through at least a first high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock;

a second microprocessor comprising one or more interfacing logics including a second interfacing logic, the second microprocessor being clocked by a third system clock;

the second microprocessor coupled to the memory controller through at least a second high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a second signal from the memory controller to the second interfacing logic, the second high frequency, point-to-point, unidirectional, source-clocked bus requiring a first period of time more to transmit the second signal than what the first high frequency, point-to-point, unidirectional, source-clocked bus requires to transmit the first signal; and

wherein the first interfacing logic is configured to delay the first signal by a second period of time and the second interfacing logic is configured to delay the second signal by a third

period of time so that the first signal and the second signal are respectively received by the first microprocessor and the second microprocessor substantially at the same time.

20. (New) The system as recited in Claim 19, wherein the memory controller further comprises one or more interfacing logics including a third interfacing logic and a fourth interfacing logic, and further comprising:

a third high frequency, point-to-point, unidirectional, source-clocked bus coupled to the memory controller and the first microprocessor and configured to transmit at least a third signal from the first microprocessor to the third interfacing logic;

a fourth high frequency, point-to-point, unidirectional, source-clocked bus coupled to the memory controller and the second microprocessor and configured to transmit at least a fourth signal from the second microprocessor to the fourth interfacing logic, the fourth high frequency, point-to-point, unidirectional, source-clocked bus requiring a fourth period of time more to transmit the fourth signal than what the third high frequency, point-to-point, unidirectional, source-clocked bus requires to transmit the third signal; and

wherein the third interfacing logic is configured to delay the third signal by a fifth period of time and the fourth interfacing logic is configured to delay the fourth signal by a sixth period of time so that the third signal and the fourth signal are respectively received by the memory controller substantially at the same time.